What is Claimed is:

1. A tamper detection system for securing a protected integrated circuit from attack, the tamper detection system comprising:

a power source;

a trigger circuit including a plurality of resistors and a plurality of wire loops, the plurality of resistors including a first resistor, a second resistor and a third resistor, all of which being wired together in series and operatively connected to the power source, the plurality of wire loops including a first wire loop extending between the first resistor and the second resistor and a second wire loop extending between the second resistor and the third resistor, the first wire loop and the second wire loop being electrically isolated from each other but in physical proximity to each other so as to form a protective mesh that envelopes the protected integrated circuit; and

a detection circuit being in operative communication with the trigger circuit and the protected integrated circuit, the detection circuit monitoring a flow of current through the trigger circuit, wherein if the flow of current through the trigger circuit is altered because of an open condition in the first wire loop or the second wire loop or a short between the first wire loop and the second wire loop, then the detection circuit outputs a predetermined signal at a designated node.

2. The tamper detection system of claim 1, further comprising:

a ground layer in physical proximity to the first wire loop or the second wire loop; and

wherein if the first wire loop or the second wire loop are shorted to the ground layer, then the detection circuit outputs the predetermined signal.

3. The tamper detection system of claim 2, wherein:

the detection circuit includes a first transistor and a second transistor,

the first transistor is operatively connected across the second resistor so that the first transistor is allowed to develop a bias voltage cross the second resistor, the second transistor is operatively connected across the first transistor and ground so that the second transistor is activated by an output current received from the first transistor, and the designated node is located between the power source and the second transistor.

4. The tamper detection system of claim 3, wherein:
the detection circuit further includes a forth resistor connected between the power source and the second transistor;
the first transistor is a PNP type having an emitter node, a base node and a collector node, the first transistor emitter node is connected between the first resistor and the second resistor, the first transistor base node is connected between the second resistor and the third resistor;
the second transistor is a NPN type having an emitter node, a base node and a collector node, the second transistor base node is connected to the first transistor collector node, the second transistor emitter node is connected to ground, the second transistor collector node is connected to the forth resistor; and
the designated node is between the forth resistor and the second transistor collector node.

5. The tamper detection system of claim 4, wherein:
the predetermined signal is a high voltage condition substantially equal to the power source.

6. The tamper detection system of claim 1, wherein:
the detection circuit includes a first transistor and a second transistor, the first transistor is operatively connected across the second resistor so that the first transistor is allowed to develop a bias voltage cross the second resistor, the second transistor is

operatively connected across the first transistor and ground so that the second transistor is activated by an output current received from the first transistor, and the designated node is located between the power source and the second transistor.

7. The tamper detection system of claim 6, wherein:

the detection circuit further includes a forth resistor connected between the power source and the second transistor;

the first transistor is a PNP type having an emitter node, a base node and a collector node, the first transistor emitter node is connected between the first resistor and the second resistor, the first transistor base node is connected between the second resistor and the third resistor;

the second transistor is a NPN type having an emitter node, a base node and a collector node, the second transistor base node is connected to the first transistor collector node, the second transistor emitter node is connected to ground, the second transistor collector node is connected to the forth resistor; and

the designated node is between the forth resistor and the second transistor collector node.

8. The tamper detection system of claim 7, wherein:

the predetermined signal is a high voltage condition substantially equal to the power source.

9. A method of producing a tamper detection system for securing a protected integrated circuit from attack, the method comprising the step(s) of:

providing a power source;

providing a trigger circuit including a plurality of resistors and a plurality of wire loops, the plurality of resistors including a first resistor, a second resistor and a third resistor, all of which being wired together in series and operatively connected to the power source, the plurality of wire loops including a first wire loop extending

between the first resistor and the second resistor and a second wire loop extending between the second resistor and the third resistor;

keeping the first wire loop and the second wire loop electrically isolated from each other;

placing the first wire loop and the second wire loop in physical proximity to each other so as to form a protective mesh that envelopes the protected integrated circuit; and

providing a detection circuit in operative communication with the trigger circuit and the protected integrated circuit, the detection circuit monitoring a flow of current through the trigger circuit, wherein if the flow of current through the trigger circuit is altered because of an open condition in the first wire loop or the second wire loop or a short between the first wire loop and the second wire loop, then the detection circuit outputs a predetermined signal at a designated node.

10. The method of claim 9, further comprising the step(s) of:

providing a ground layer in physical proximity to the first wire loop or the second wire loop; and

wherein if the first wire loop or the second wire loop are shorted to the ground layer, then the detection circuit outputs the predetermined signal.

11. The method of claim 10, wherein:

the detection circuit includes a first transistor and a second transistor, the first transistor is operatively connected across the second resistor so that the first transistor is allowed to develop a bias voltage across the second resistor, the second transistor is operatively connected across the first transistor and ground so that the second transistor is activated by an output current received from the first transistor, and the designated node is located between the power source and the second transistor.

12. The method of claim 11, wherein:

the detection circuit further includes a forth resistor connected between the power source and the second transistor;

the first transistor is a PNP type having an emitter node, a base node and a collector node, the first transistor emitter node is connected between the first resistor and the second resistor, the first transistor bias node is connected between the second resistor and the third resistor;

the second transistor is a NPN type having an emitter node, a base node and a collector node, the second transistor base node is connected to the first transistor collector node, the second transistor emitter node is connected to ground, the second transistor collector node is connected to the forth resistor; and

the designated node is between the forth resistor and the second transistor collector node.

13. The method of claim 12, wherein:

the predetermined signal is a high voltage condition substantially equal to the power source.

14. The method of claim 9, wherein:

the detection circuit includes a first transistor and a second transistor, the first transistor is operatively connected across the second resistor so that the first transistor is allowed to develop a bias voltage across the second resistor, the second transistor is operatively connected across the first transistor and ground so that the second transistor is activated by an output current received from the first transistor, and the designated node is located between the power source and the second transistor.

15. The method of claim 14, wherein:

the detection circuit further includes a forth resistor connected between the power source and the second transistor;

the first transistor is a PNP type having an emitter node, a base node and a collector node, the first transistor emitter node is connected between the first resistor and the second resistor, the first transistor base node is connected between the second resistor and the third resistor;

the second transistor is a NPN type having an emitter node, a base node and a collector node, the second transistor base node is connected to the first transistor collector node, the second transistor emitter node is connected to ground, the second transistor collector node is connected to the forth resistor; and

the designated node is between the forth resistor and the second transistor collector node.

16. The method of claim 15, wherein:

the predetermined signal is a high voltage condition substantially equal to the power source.

17. A method of detecting an attempt to tamper with a protected integrated circuit, the method comprising the step(s) of:

providing a power source;

providing a trigger circuit including a plurality of resistors and a plurality of wire loops, the plurality of resistors including a first resistor, a second resistor and a third resistor, all of which being wired together in series and operatively connected to the power source, the plurality of wire loops including a first wire loop extending between the first resistor and the second resistor and a second wire loop extending between the second resistor and the third resistor;

keeping the first wire loop and the second wire loop electrically isolated from each other;

placing the first wire loop and the second wire loop in physical proximity to each other so as to form a protective mesh that envelopes the protected integrated circuit;

providing a detection circuit in operative communication with the trigger

circuit and the protected integrated circuit, the detection circuit monitoring a flow of current through the trigger circuit; and

if the flow of current through the trigger circuit is altered because of an open condition in the first wire loop or the second wire loop or a short between the first wire loop and the second wire loop, then outputting a predetermined signal at a designated node of the detection circuit.

18. The method of claim 17, further comprising the step(s) of:

providing a ground layer in physical proximity to the first wire loop or the second wire loop; and

if the first wire loop or the second wire loop are shorted to the ground layer, then outputting the predetermined signal.

19. The method of claim 18, wherein:

the detection circuit includes a first transistor and a second transistor, the first transistor is operatively connected across the second resistor so that the first transistor is allowed to develop a bias voltage across the second resistor, the second transistor is operatively connected across the first transistor and ground so that the second transistor is activated by an output current received from the first transistor, and the designated node is located between the power source and the second transistor.

20. The method of claim 19, wherein:

the detection circuit further includes a forth resistor connected between the power source and the second transistor;

the first transistor is a PNP type having an emitter node, a base node and a collector node, the first transistor emitter node is connected between the first resistor and the second resistor, the first transistor base node is connected between the second resistor and the third resistor;

the second transistor is a NPN type having an emitter node, a base

node and a collector node, the second transistor base node is connected to the first transistor collector node, the second transistor emitter node is connected to ground, the second transistor collector node is connected to the forth resistor; and

the designated node is between the forth resistor and the second transistor collector node.

21. The method of claim 20, wherein:

the predetermined signal is a high voltage condition substantially equal to the power source.

22. The method of claim 17, wherein:

the detection circuit includes a first transistor and a second transistor, the first transistor is operatively connected across the second resistor so that the first transistor is allowed to develop a bias voltage across the second resistor, the second transistor is operatively connected across the first transistor and ground so that the second transistor is activated by an output current received from the first transistor, and the designated node is located between the power source and the second transistor.

23. The method of claim 22, wherein:

the detection circuit further includes a forth resistor connected between the power source and the second transistor;

the first transistor is a PNP type having an emitter node, a base node and a collector node, the first transistor emitter node is connected between the first resistor and the second resistor, the first transistor base node is connected between the second resistor and the third resistor;

the second transistor is a NPN type having an emitter node, a base node and a collector node, the second transistor base node is connected to the first transistor collector node, the second transistor emitter node is connected to ground, the second transistor collector

node is connected to the forth resistor; and

the designated node is between the forth resistor and the second transistor collector node.

24. The method of claim 23, wherein:

the predetermined signal is a high voltage condition substantially equal to the power source.